

# Survey on High speed folding and interpolation ADC in CMOS technology

<sup>1</sup>Rahul Kumar Baghel, <sup>2</sup>Braj Bihari Soni

<sup>1,2</sup>,NRI Institute of Information Science & Technology, Bhopal, MP, India

**Abstract:-** Folding and interpolation ADC has been shown to be an important means of digitization of high BW signals at intermediate resolution. The objective of this paper is to design and identify the performance of the ADC. Flash ADC is one of the faster ways to convert any analog signal to a digital signal. It uses folding and interpolating techniques allow each comparator of the ADC to be reused several times over the full scale input range. In addition interpolating technique can reduce the number of folding circuit required in a folding ADC hence further improve the performance of the ADC in term of capacitive loading and power consumption .

**Keyword:-** Flash ADC, Folding and interpolation, comparator , Folding amplifier.

## I. Introduction

The best known architecture for a high speed analog to digital converter structure. In this structure an array of comparators compares the input voltage with asset of increasing reference voltages. The comparator outputs represents the input signal in a digital (thermometer) code which can be easily converted into a gray code or binary weighted output code[1,3]. The flash ADC shows a good speed performance and can easily be implemented in an integrated

circuit as a repetition of simple comparator blocks and a decoder structure.

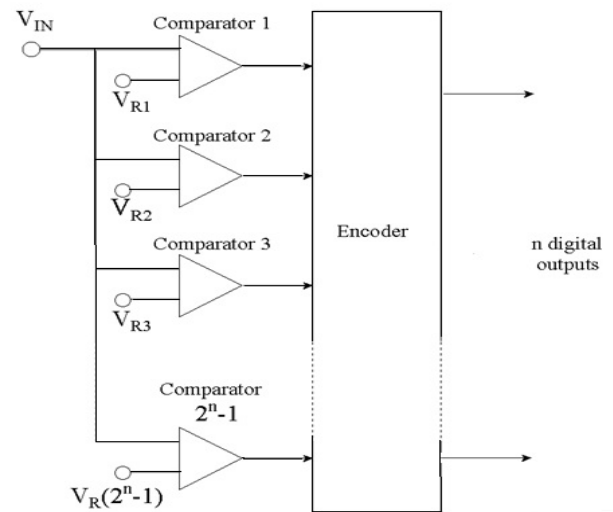


Fig.1 Full Flash ADC

However this architecture requires  $2^N-1$  comparators to achieve an N-bit resolution. The parallel structure makes it difficult to obtain a high resolution while maintaining at the same time a large bandwidth, a low power consumption and a small die size[6].

## II. Overview of Important Term

**Folding:** - The concept of folding ADC converter was first introduced by Arbel and Kurz in 1975. The main motivation was the dramatic reduction of the number of comparators required in the design. The transfer function of the folding circuit is

given. The I/O characteristics of folding circuit can be parameterized by number of folds. This parameter determines resolution of both coarse and fine ADC [4].

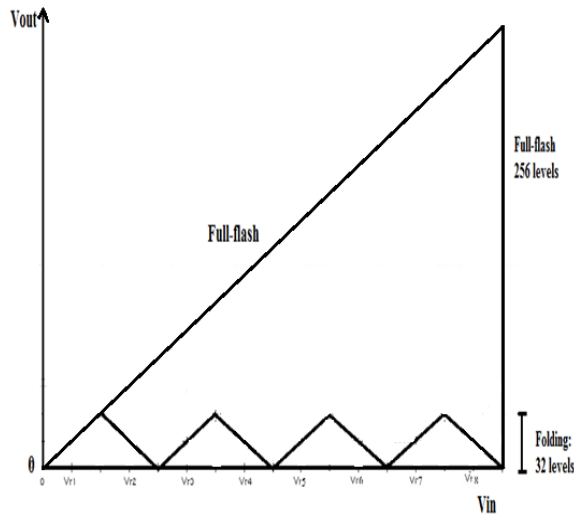


Fig.2 Ideal folding transfer function in comparison with that of a flash ADC

**Interpolation:-** Interpolation is often employed to generate extra folding waveforms without increasing number of folding amplifiers.

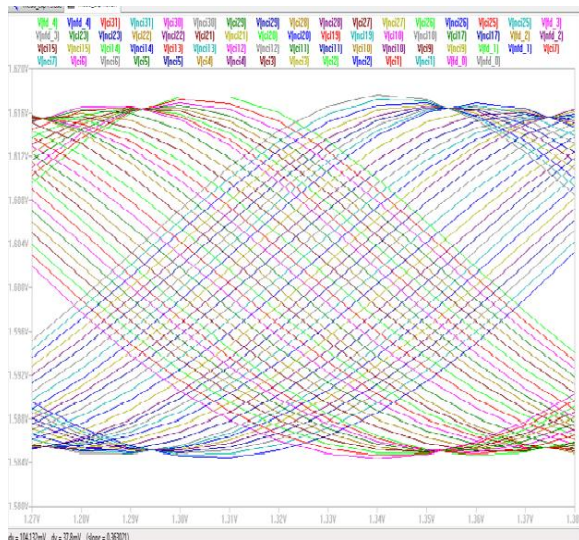


Fig 3 interpolation of signal

There are basically two methods to interpolate the folded signals, namely voltage-mode (resistive) interpolation and current-mode interpolation. The current mode interpolation is based on summation of currents reflected through current mirrors with different ratios. It proves to be power hungry and not very precise due to the non-idealities of the current mirrors.

### III. Literature Review

1. In 2012 Wan Rosmaria wan, ahmad, Ifzuan Mazlan presented a High speed with low power folding and interpolating ADC using two types of comparator in CMOS 0.180um technology compares the performance of two different comparator using conventional folding amplifier. CMOS folding provides eight times folding factor for whole analog input range by using 12 differential amplifier that are differentially connected.

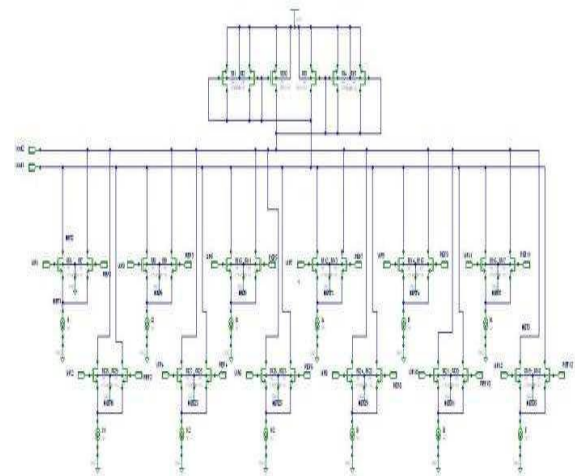


Fig.4 CMOS folding circuit

In this paper low power high folding factor blocks are implemented by several low power five-level folders. The design is simulated using 0.18um technology and can

operate in low power which is 2V of power supply, 2GHz of input frequency and 0.59202W of power consumption based to gateway SDA tools simulation result.

2 .In 2011 Vinayashree Hiremath, Saiyu Ren member of IEEE presented A 6-bit low power folding and interpolating ADC. This circuit consists of mainly the folding circuit, zero crossing detectors [ZCD] and a digital encoder. The folding circuit and ZCD are used to convert cyclic thermometer code to binary. The design of resistor in interpolation block and ZCD are vital in achieving desired bandwidth. As the coarse and fine bits are generated separately a major challenge lies in the design of synchronization circuit to obtain accurate results

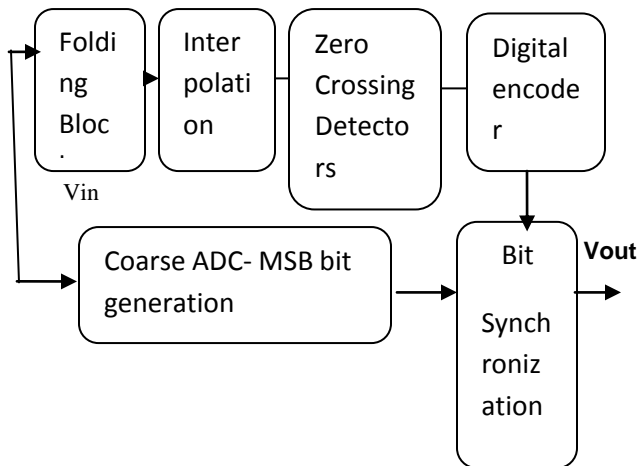


Fig.5 Block diagram of 6-bit folding and interpolating ADC

Here a unique 6 bit ADC which has optimum performance at sampling frequency of 400MHz is designed and simulated successfully in 90nm technology.

3. In 2011 Shruti Oza, N.M. Devashrayee presented a Low power folding and

interpolating ADC using 0.35-um technology. The pre processing block-folding amplifier is designed to reduce power consumption and settling time. In ADC, comparators consume the major part of the total power. The converter architecture is designed with reduced number of comparators and minimum hardware. For further reduction of latency and number of comparators, folding amplifier is used in the design of coarse and fine converter both.

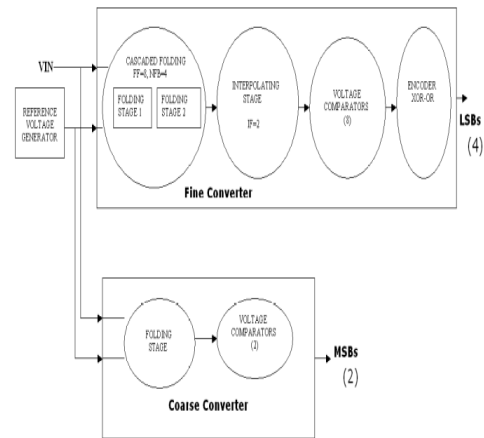


Fig. 6 Block diagram of 6- ADC

To reduce the power consumption, encoder based on XOR-OR logic is used. The post simulation results are obtained using 0.35um technology at 3.3V.

4. In 2010 Shruti K. Oza, N.M. Devashrayee presented a low power and interpolating ADC using 0.18um technology. The folding amplifier can be used to produce more than one zero-crossing point to reduce required number of comparators. The converter is designed using novel low voltage, low power folding amplifier with folding factor=4. The folding amplifier is used in the design of coarse and fine converter both.

To reduce the power consumption, encoder based on XOR-OR logic is used. The design is implemented using 0.18µm technology at 1.7V supply voltage.

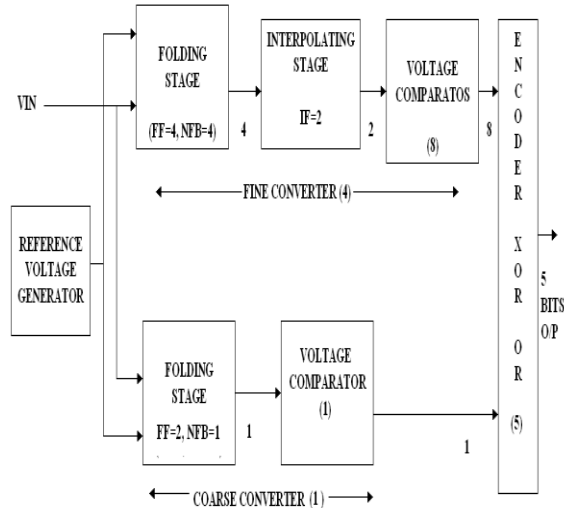


Fig.7 Block diagram of 5-bit folding & interpolating ADC

The architecture uses folding pre-processing circuit for both coarse & fine converter. To achieve low power operation, folding block, comparator & encoder are optimized. The design is simulated using 0.18µm technology at 1.7V. The simulation results indicate that the design achieves low power operation. Due to cyclic output of folding block comparison, number of comparators required is only 9. The design also helps in reducing latency difference of coarse and fine converter.

5. In 2009 Shruti Oza, presented Low Voltage, Low Power Folding Amplifier for Folding & Interpolating ADC. This paper presents simple low voltage, low power folding amplifier with folding factor=4 for folding and interpolating ADC. The design is implemented using 0.13µm technology at 1.5V supply voltage.

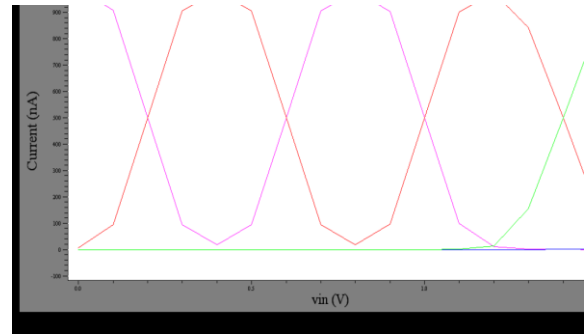


Fig.8 DC Characteristics of Low Voltage, Low Power Folding Amplifier

The simulation results are compared with voltage mode (conventional differential pair based) folding amplifier and current steering folding amplifier. All three folding amplifiers are simulated using 0.13-µm technology, 1.5V supply voltage. The value of current source and size of transistors in all three designs are chosen same. Due to multiple current sources, it is obvious that Voltage Mode Folding Amplifier consumes more power.

#### IV. Research Objective

The architecture of a 8-bit folding and interpolation is shown in fig.

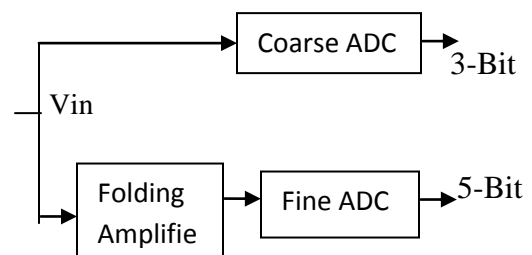


Fig.9 Folding and Interpolation ADC  
In above diagram I want to replace conventional folding amplifier. Because in my base paper they used conventional folding amplifier, which suffers from mismatch between several current sources

and the excessive capacitive loading at the output of folding amplifier. To alleviate the problem in the conventional folding amplifier, a current steering folding amplifier has been developed. Implement layout for complete design using linear technology spice tools.

## V. Conclusion & Future Scope

The low power, medium resolution folding and interpolating ADC design is intricate. An efficient folding circuit with differential output voltage constitutes the analog preprocessing block and is core to this ADC. Current steering folding amplifier is more efficient than conventional folding amplifier. The design of resistor in interpolation block and ZCD are vital in achieving desired bandwidth.

As the coarse and fine bits are generated separately a major challenge lies in the design of synchronization circuit to obtain accurate results.

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